LOW NOISE MICROWAVE HIFET USING MOCVD

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Abstract

Low noise HIFET (Hetero Interface Field Effect Transistor, also known as TEGFET or HEMT) AlGaAs/GaAs heterostructure devices have been developed using Metal Organic Chemical Vapor Deposition (MOCVD).

The HIFET's with 0.5-micron long and 200-micron wide gates have shown a minimum noise figure of 0.87 dB with an associated gain of 12.5 dB at 12 GHz at room temperature. A substantial improvement in noise figure was obtained at lower temperatures (-10°C), especially when compared to GaAs MESFET devices.

Introduction

To meet the ever-increasing demands for low noise, high performance microwave circuits, development of low noise devices for front end amplifiers is being actively pursued [1],[2].

The limits of performance attainable using GaAs MESFET's are being approached by means of fine-pattern lithography and optimization of various device parameters. HIFET devices using AlGaAs/GaAs heterojunctions have displayed performance surpassing GaAs MESFET's within a short development period [3]. The heterojunction epitaxy for low noise HIFET's has so far been performed using MBE (Molecular Beam Epitaxy) by virtue of the high quality of the epitaxial interface.

We have previously reported on the first fabrication of low noise HIFET's using MOCVD which has superior wafer throughput and surface quality (NF=1.4dB, Ga=9dB @ 12GHz) [4].

In this paper we will report on improvements made in the original device performance by means of modifications in the heterojunction epitaxy, optimization of the device pattern, and reduction of the gate length to 0.5 microns. An NF of 0.87 dB and a Ga of 12.5 dB were measured at room temperature.

Device Fabrication

The epitaxial layers for the formation of the heterojunctions are grown by MOCVD using trimethyl organometallics (TMA and TMG) and AsH_3 under atmospheric pressure. The growth temperature is 720°C and the growth rate is about 240 Å/min.

Hall mobilities of the two dimensional electron gas at the interface are 8030 and 148000 cm^2/V-sec at 300 and 77 K, respectively, with an undoped $Al_{0.3}Ga_{0.7}As$ spacer layer of 100Å.

The mobility and the sheet carrier concentration of the two dimensional electron gas (2DEG) are comparable to those reported using MBE.

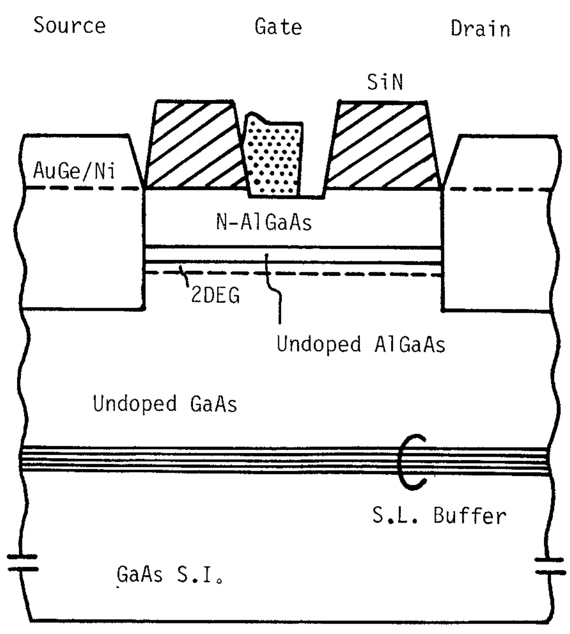


Figure 1. Cross section of low noise HIFET using MOCVD

A high mobility and a low sheet resistivity of the 2DEG are the most important parameters for realizing low noise HIFET's.

A high mobility of the 2DEG is desirable for low noise operation, while a low sheet resistivity is required for reducing the source resistance. A thin superlattice buffer of alternating undoped AlAs and GaAs layers and a 10Å-thick undoped AlGaAs spacer layer were introduced to respond to the above requirements as shown in the device cross section of Figure 1. The 2DEG of the actual device showed a mobility of 5400 cm^2/V-sec and a sheet resistivity of 800 ohms/square. When cooled to 77 K, the mobility increased to 26000 cm^2/V-sec.

The low noise HIFET devices are fabricated on 2-inch [100] epitaxial wafers using standard UV contact photolithography.

The gate metal is evaporated at an angle such that the gate is offset towards the source. This makes possible the reduction in the effective gate length together with a decrease in the series gate resistance resulting from the gate's cross section.

These modifications to the epitaxial structure together with the gate definition processing contributes to the reduction in the noise figure, which mainly depends on the gate-to-source series resistance and the gate length as expressed in Fukui's equation. The gate length is less than 0.5 microns and the source-to-drain spacing is 3 microns.

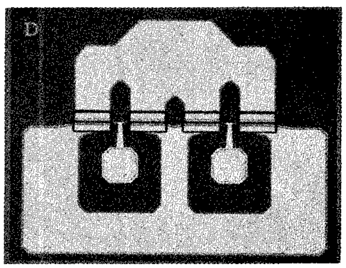
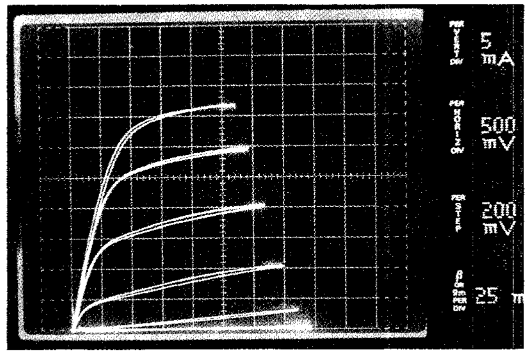
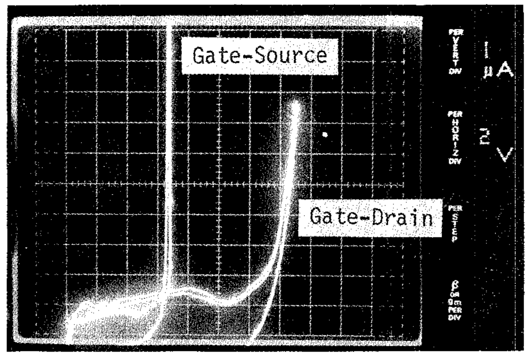


Figure 2. Chip photograph of low noise HIFET



(a)



(b)

Figure 3. DC characteristics of HIFET
(a) Drain I/V characterisics
(b) Gate schottky breakdown characteristics

DC and RF Performance

The typical drain current characteristics and the gate schottky breakdown characteristics of HIFET's having a gate length of 0.5 microns and gate width of 200 microns are shown in Figure 3(a),3(b), respectively. At 300 K, the maximum extrinsic transconductance was 280 mS/mm at a current density of 120 mA/mm. The intrinsic transconductance calculated from the source resistance was found to have a value of 360 mS/mm. Since the source resistance mainly consists of the 2DEG element between the gate and source, reducing the gate-to-source spacing and decreasing the 2DEG sheet resistance (by increasing the sheet carrier density and mobility) will make possible an even higher extrinsic transconductance than the above value.

Under actual use, the gate Schottky breakdown characteristic is an important parameter comparable to all others. Generally, a lower breakdown voltage of the gate Schottky is achieved with HIFET's compared to GaAs MESFET's because of the high donor density in the AlGaAs layer. As shown in Figure 3(b), the typical breakdown voltage values of gate-to-source and gate-to-drain are >5 V and >10 V, respectively. Increasing the gate-to-drain breakdown voltage has been accomplished by means of offsetting the gate metal towards the source and optimizing the gate pinch-off voltage, thereby reducing the electric field strength present across the gate and drain. These values are comparable to those of GaAs MESFET's. An analytical model based on Fukui's equation [5], taking the parasitic capacitances of the gate bonding pads into consideration, have been developed as a guide in optimizing the HIFET device performance. The number of gate bonding pads determines the equivalent gate series resistance and the input capacitance, which in turn determines the noise figure and gain.

Using the above factors in the design of the device pattern layout, it was decided that with a gate width of 200 microns, optimum device performance will be achieved using two bonding pads as shown in Figure 2.

For microwave evaluations, the low noise HIFET chips were mounted on 1.8 mm square ceramic packages. Noise figures and associated gains were measured at 12 GHz using conventional slide tuners. The drain voltage was set at 2.0 V which results in the best noise figure. The dependence of noise figure and associated gain on drain current is shown in Figure 4. Noise figure values under 1.0 dB were obtained at drain currents between 6 mA and 10 mA at room temperature. The minimum noise figure was 0.87 dB with an associated gain of 12.5 dB at a drain current of 8 mA. These results are comparable to other previously reported HIFET's, having quarter-micron gate lengths fabricated by direct-write electron beam (EB) lithography on epitaxial layers grown by MBE [6],[7].

The noise figure circles of Figure 5 show that the HIFET is capable of very broadband operation, having a 50-ohm unmatched noise figure of 1.77 dB. This value is about 1.0 dB better than that of a conventional MESFET. Thus, the HIFET is more tolerant of input mismatching, and is suited for wideband MMIC designs. S-parameter measurements indicate that the HIFET has similar input/output impedance characteristics to a MESFET, thus assuring a high degree of compatibility. The high transconductance of the HIFET results in an fmax of 70 GHz.

In addition to 12 GHz noise performance measured at room temperature, the devices were thermoelectrically cooled down to $-20^{\circ}C$ in order to measure the temperature dependence [8].

As shown in Figure 6, the HIFET's have shown a larger dependence ($0.1dB/20^{\circ}C$) than that of the MESFET's ($0.05dB/20^{\circ}C$) at a temperature around $10^{\circ}C$. (The HIFET's used in this experiment were selected for matched performance at room temperature with the MESFET's for comparison purposes.)

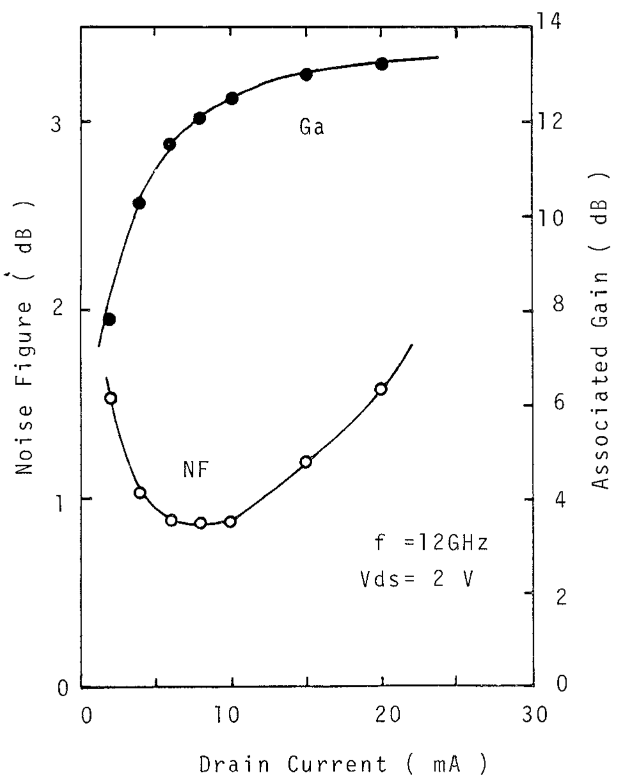


Figure 4. Noise figure and associated gain as a function of drain current

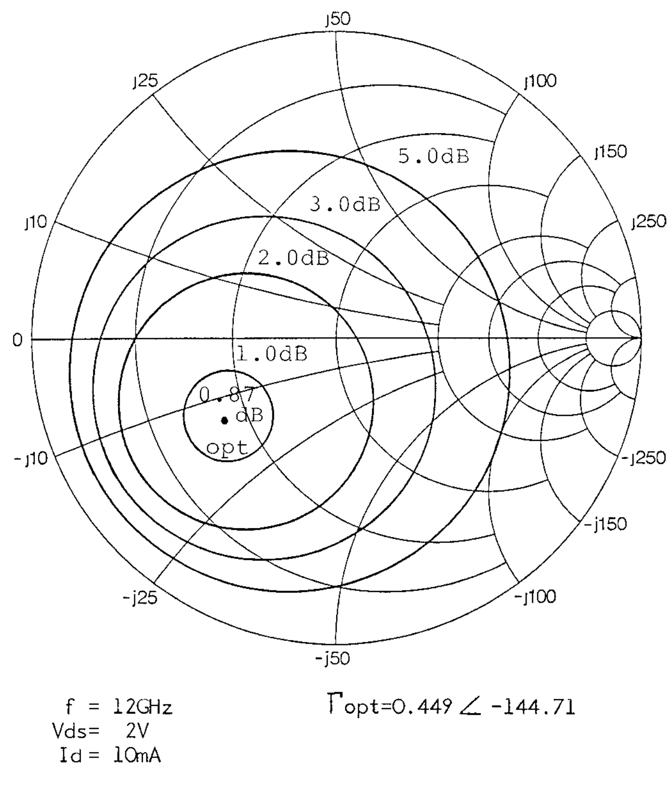


Figure 5. Γ opt and noise figure circles of low noise HIFET

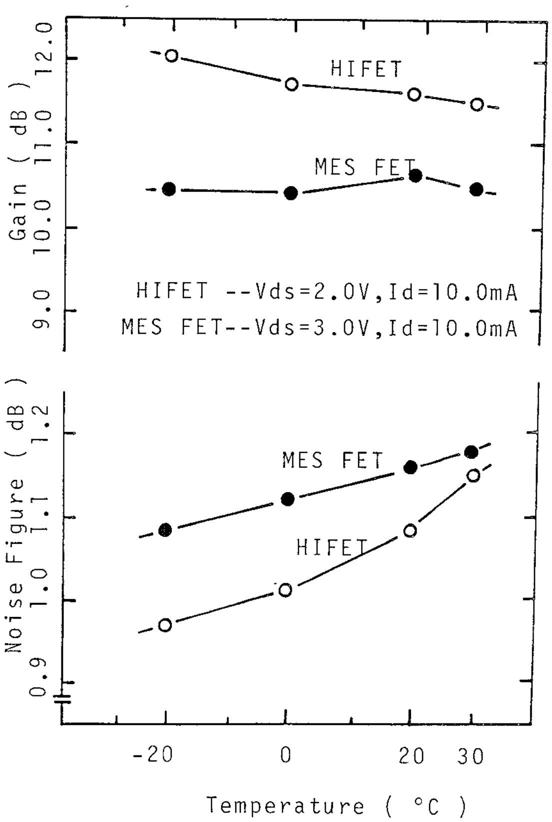


Figure 6. Temperature dependence of noise figure and associated gain of HIFET and MESFET

Conclusion

Low noise HIFET's fabricated using AlGaAs/GaAs hetero interface structures have been successfully developed by combining standard photolithographic techniques with MOCVD technology. Excellent performance including a noise figure of 0.87 dB and associated gain of 12.5 dB at 12 GHz at room temperature have been demonstrated.

A thin superlattice buffer and a 10Å thick undoped AlGaAs layers were introduced to increase the mobility of 2DEG at the hetero interface. The gate length of less than 0.5 microns, formed by an angle evaporation lift-off technique, also contributes to an improvement in both RF performance and breakdown voltage.

Further refinements in the HIFET process technology directed at the reduction of parasitic elements will allow an even lower noise figure than those reported here.

The feasibility of high performance HIFET devices for general purpose applications based on high-productivity MOCVD process has been demonstrated.

Acknowledgement

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References

[1] K. Joshin, Y. Yamashita, M. Niori, J. Saito, T. Mimura, and M. Abe: "Low Noise HEMT with Self-Aligned Gate Structure", Extended Abstracts of the 16th conf. on Solid State Devices and Materials, 1984, pp. 347-350.

[2] M. Laviron, D. Delagebeaudeuf, J.F. Rochette, P.R. Jay, P. Delesluse, J. Chevrier and Nuyen. T. Linh: "Ultra Low Noise and High Frequency Operation of TEGFET Made by MBE", Physics 129b, 1985, pp. 376-379.

[3] K. Shibata, B. Abe, H. Kawasaki, S. Hori and K. Kamei: "Broadband HEMT and GaAS FET Amplifiers for 18-26.5 GHz", IEEE MTT-S Digest, June 1985, PP. 547-550.

[4] H. Takakuwa, Y. Kato, S. Watanabe and Y. Mori: "Low-Noise HEMT Fabricated by MOCVD", Electronics Letters 14th, Vol. 21, No. 4, February 1985, pp. 125-126.

[5] H. Fukui: "Optimal Noise Figure of Microwave GaAs MESFET's", Electron Devices, Vol. ED-26, No. 7, July 1979.

[6] M. Sholley, J. Berenz, A. Nichols, K. Nakano, R. Sawires and J. Abell: "36.0-40.0 GHz HEMT Low Noise Amplifier", IEEE MTT-S Digest, June 1985, pp. 555-558.

[7] U.K. Mishira, S.C. Palmateer, P.C. Chao, P.M. Smith and J.C.M. Hwang: "Microwave Performance of 0.25-micron Gate Length High Electron Mobility Transistors", IEEE Electron Device Letters, Vol. EDL-6, No.3, March 1985, pp.142-145.

[8] K. Kamei, S. Hori, H. Kawasaki, S. Shibata, H. Mashita and Y. Ashizawa: "Low Noise High Electron Mobility Transistor", GaAs and Related Compounds Symp. 1984, pp.545-550.